What is claimed is:

1. A semiconductor device, comprising:

an output clock signal generator for receiving a first system clock signal and generating an output clock signal having a frequency n times the frequency of the first system clock signal, where n is an integer;

an output driver for synchronizing output data with the output clock signal and outputting the synchronized output data through an input and output terminal;

a restoring clock signal generator for receiving a second system clock signal and generating a plurality of restoring clock signals having the same frequency as the frequency of the second system clock signal and each having different phases; and

a high frequency equalizer for restoring lost high frequency components of input data input through the input and output terminal in response to the restoring clock signals and outputting the restored input data.

2. A semiconductor device, as recited in claim 1, wherein the output clock signal generator comprises a phase locked loop circuit.

3. A semiconductor device, as recited in claim 1, wherein the restoring clock signal generator comprises a PLL circuit.

4. A semiconductor device, as recited in claim 1, wherein the high frequency equalizer comprises:

a restoring circuit operating in response to the restoring clock signals, for demultiplexing the input data into a plurality of input data items each having a time difference the same as a period of the input data, restoring the lost high frequency components of the plurality of demultiplexed input data items, and outputting the restored input data items; and

a multiplexer operating in response to the restoring clock signals, for multiplexing the restored input data items of the restoring circuit and sequentially outputting the multiplexed data items one by one as restored input data.

5. A semiconductor device, as recited in claim 4, wherein the restoring circuit comprises:

a demultiplexer for demultiplexing the input data into the plurality of input data items; and

a plurality of unit restoring circuits, each operating to receive a current input data item of a current period of time and a previous input data item of a previous period of time from among the plurality of input data items, restoring the lost high frequency component of the current input data item to form a restored input data item, and outputting the restored input item in response to a corresponding one of the restoring clock signals.

6. A semiconductor device, as recited in claim 5, wherein each of the unit restoring circuits comprises:

a restoring cell for receiving the current input data item the previous input data item and restoring the lost high frequency component of the current input data to form an intermediate input data item; and

a latch circuit operating in response to the corresponding restoring clock signal, for storing and amplifying the intermediate input data item, and outputting the amplified intermediate input data item as the restored input data item.

7. A semiconductor device, as recited in claim 6, wherein the restoring cell comprises:

a regular current source for supplying a first source current;

a compensation current source for providing a second source current;

a first current amplifying circuit for amplifying the first source current in response to the current input data item and a reference voltage;

a second current amplifying circuit for amplifying the second source current in response to the previous input data item and the reference voltage;

a first current output transistor commonly connected to a first output terminal of the first current amplifying circuit and a second output terminal of the second current

amplifying circuit, for outputting a first comparison current proportional to the difference between the currents output from the first and second output terminals; and

a second current output transistor commonly connected to a third output terminal of the first current amplifying circuit and a fourth output terminal of the second current amplifying circuit, for outputting a second comparison current proportional to the difference between the currents output from the third and fourth output terminals.

8. A semiconductor device, as recited in claim 7, wherein the second source current is equal to the first source current times an interference signal of the previous input data item.

9. A semiconductor device, as recited in claim 6, wherein the latch circuit comprises:

a first switching unit for transmitting the output of the restoring cell in response to the corresponding restoring clock signal;

a first latch for amplifying and storing the output of the restoring cell transmitted through the first switching unit as a first stored data item;

a second switching unit for transmitting the first stored data item in response to an inverted clock signal of the corresponding restoring clock signal; and

a second latch for amplifying and storing the first stored data item transmitted through the second switching unit as a second stored data item, and outputting the second stored data item as the restored input data item.

10. A semiconductor device, as recited in claim 1, further comprising an inner clock signal generator for receiving one of the plurality of restoring clock signals and generating an internal clock signal having a frequency equal to m times the frequency of the received restoring clock signal, wherein m is an integer.

11. A high frequency equalizer, comprising:

a restoring circuit for demultiplexing input data into a plurality of input data items each having a time difference the same as period of the input data, restoring lost high frequency components of the plurality of demultiplexed input data items, and outputting restored input data items in response to restoring clock signals; and

a multiplexer for multiplexing the restored input data items and sequentially outputting multiplexed data items one by one as restored input data, in response to the restoring clock signals.

12. A high frequency equalizer, as recited in claim 11, wherein the restoring circuit comprises:

a demultiplexer for demultiplexing the input data into the plurality of input data items in response to the restoring clock signals; and

a plurality of unit restoring circuits operating in response to the corresponding restoring clock signal, for receiving current input data items of a current time and previous input data of a previous period of time, restoring the lost high frequency component of the current input data item, and outputting restored input data items.

13. A high frequency equalizer, as recited in claim 12, wherein the unit restoring circuit comprises:

a restoring cell for receiving the current input data item and the previous input data item and restoring the lost high frequency component of the current input data item to form an intermediate input data item; and

a latch circuit for storing and amplifying the intermediate input data item in response to the corresponding restoring clock signal and outputting the amplified intermediate data item as a restored input data item.

14. A high frequency equalizer, as recited in claim 13, wherein the restoring cell comprises:

a regular current source for supplying a first source current;

a compensation current source for providing a second source current;

a first current amplifying circuit for amplifying the first source current in response to the current input data item and a reference voltage;

a second current amplifying circuit for amplifying the second source current in response to the previous input data item and the reference voltage;

a first current output transistor commonly connected to a first output terminal of the first current amplification circuit and to a second output terminal of the second current amplification circuit, for outputting a current proportional to the difference between the currents output first and second output terminals; and

a second current output transistor commonly connected to a third output terminal of the first current amplifying circuit and a fourth output terminal of the second current amplifying circuit, for outputting a current proportional to the difference between the currents output from the third and fourth output terminals.

15. A high frequency equalizer, as recited in claim 13, wherein the latch circuit comprises:

a first switching unit for transmitting the intermediate data item from the restoring cell in response to the corresponding restoring clock signal;

a first latch for amplifying and storing the intermediate input data item as a first stored data item;

a second switching unit for transmitting the first stored data item in response to an inverted clock signal of the corresponding restoring clock signal; and

a second latch for amplifying and storing the first stored data item as a second stored data item, and outputting the second stored data item as a restored input data item.

16. A unit restoring circuit, comprising:

a regular current source for supplying a first source current;

a compensation current source for providing a second source current;

a first current amplifying circuit for amplifying the first source current in response to a current input data item and a reference voltage;

a second current amplifying circuit for amplifying the second source current in response to a previous input data item and the reference voltage;

a first current output transistor commonly connected to a first output terminal of the first current amplifying circuit and a second output terminal of the second current amplifying circuit, for outputting a first difference current proportional to the difference between the currents output from the first and second output terminals; and

a second current output transistor commonly connected to a third output terminal of the first current amplifying circuit and a fourth output terminal of the second current amplifying circuit, for outputting a second difference current proportional to the difference between the currents output from the third and fourth output terminals.

17. A unit restoring circuit, as recited in claim 16, wherein the first current amplifying circuit comprises:

a first PMOS transistor having a first source connected to the current source, a first gate connected to the current input data item, and a first drain connected to the first current output transistor and forming the first output terminal; and

a second PMOS transistor having a second source connected to the current source, a second gate connected to the reference voltage, and a second drain connected to the second current output transistor and forming the third output terminal.

18. A unit restoring circuit, as recited in claim 16, wherein the second current amplifying circuit comprises:

a third PMOS transistor having a third source connected to the compensation current source, a third gate connected to the previous input data item, and a third drain connected to the second current output transistor and forming the second output terminal; and

a fourth PMOS transistor having a fourth source connected to the compensation current source, a fourth gate connected to the reference voltage, and a fourth drain connected to the first current output transistor and forming the fourth output terminal.

19. A unit restoring circuit, as recited in claim 16, wherein the first current output transistor is a first NMOS transistor having a first drain and a first gate commonly connected to the first and second output terminals, and having a first source connected to a ground voltage.

20. A unit restoring circuit, as recited in claim 16, wherein the second current output transistor is a second NMOS transistor having a second drain and a second gate commonly connected to the third and fourth output terminals, and having a second source connected to a ground voltage.

21. A unit restoring circuit, as recited in claim 16, further comprising a latch circuit operating in response to a restoring clock signal, for storing and amplifying the first and second difference currents, and outputting the amplified current outputs.

22. A unit restoring circuit, as recited in claim 21, wherein the latch circuit comprises:

a first switching unit for transmitting first and second outputs of the first and second current output transistors in response to the restoring clock;

a first latch for amplifying and storing the first and second outputs of the first and second current output transistors transmitted through the first switching unit;

a second switching unit for transmitting the output of the first latch in response to an inverted clock signal of the of the restoring clock signal; and

a second latch for amplifying and storing the output of the first latch transmitted through the second switching unit and outputting it as restored output data.